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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/708,342 | 02/25/2004 | Michael L. Combs | BUR920030200US1 | 2341 |

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| EXAMINER | |
|---|---|
| ABRAHAM, ESAW T | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2133 | |

DATE MAILED: 09/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/708,342 | COMBS ET AL. | |
| | Examiner | Art Unit | |
| | Esaw T. Abraham | 2133 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-20 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 21 February 2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 02/25/04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

1. Claims **1-20** are presented for examination.

### *Information Disclosure Statement*

2. The references listed in the information disclosure statement submitted on 08/19/99 have been considered by the examiner (see attached PTO-1449).

### *Specification*

3. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

### *Claim objections*

4. Claim **1-20** are objected to because of the following informalities:

a) The numbering of claims is not in accordance with 37 CFR 1.126 which requires the original numbering of the claims to be preserved throughout the prosecution. When claims are canceled, the remaining claims must not be renumbered. When new claims are presented, they must be numbered consecutively beginning with the number next following the highest numbered claims previously presented (whether entered or not). Please renumber claim 12 to read as claim 11.

b) Please change "Shmoo testing said memory array by incrementing, decrementing or decrementing and decrementing values" to ---shmoo testing said memory array by incrementing and decrementing values--- (see claim 1 line 8 and 9).

c) The claims (1, 6, 10 and 14) are not indented properly, making reading and entry of amendments difficult. Substitute claims with proper indentation, lines one and one-half or double spaced on good quality paper are required. See 37 CFR 1.52(b).

Correction is required.

***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U. S. C 112

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

5. Claims **1, 2, 10 and 11** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a) Claims 1 and 10 recites the limitation "shmoo testing and minimum or maximum value of said test parameter " is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one ordinary skill in the art would not be reasonably appraise of the scope of the invention. The examiner would appreciate if the applicant would clarify this matter.

b) Claims 2 and 11 recite the limitation "first number of fuses plus said second number of fuses equal said total number of fuses or said first number of fuses plus said second number of fuses equal said total number of fuses minus a predetermined number of fuses is in comprehensive (having subject to no limit). Further, this limitation is not clear how the first and second number of fuses compared with the total number of fuses minus a predetermined number of fuses. This limitation must be rewritten to

clearly claim what the Applicant intends. The examiner would appreciate if the applicant would clarify this matter.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere* CO., 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims **1-20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Anand et al. (U.S. PN: 6,768,694) in view of Thatcher et al. (U.S. PN: 6,795,788).

**As per claims 1and 10:**

Anand et al. teach or disclose to testing and replacing defective devices through the use of fuses and more specifically to an on-chip fuse controller that provides a uniform interface for tester access across multiple chip designs (see col. 1, lines 8-12).

Further, Anand et al. teach an invention that provides an application specific integrated circuit (ASIC) chip which has memory elements, a plurality of fuses connected to the memory elements that can be programmed to replace defective memory elements with replacement memory elements (arrays), and a fuse controller connected to the fuses that can program the fuses. The fuse controller has a standardized test interface protocol for an external tester includes a repair data processing unit adapted to initiate BIST units. The invention has repair registers connected to the BIST units, which are adapted to collect repair data relating to the defective memory elements (arrays) (see col. 2, lines 14-61). Anand et al. **do not explicitly** teach a Shmoo testing a memory array by incrementing or decrementing a test parameter. **However,** Thatcher et al. in an analogous art teach a method and apparatus for conducting a boundary search for shmoo tests on an electronic device and the method discloses the discovery of an operational range for a hardware device over a plurality of varying operating parameters wherein the operational range is discovered by testing points, as defined by the plurality of varying (decrementing and incrementing) operating parameters, to discover an operational boundary of the device (see col. 2 lines 17-32). **Therefore,** it would have been obvious to a person having an ordinary skill in the art at the time the invention was made to implement the teachings (Shmoo testing) of Thatcher et al. for testing memory array (memory elements) into the invention of Anand et al. to provide efficient reliable operation. **This modification** would have been obvious because a person having ordinary skill in the art would have been motivated to do so because it would reduce the amount of testing subjected on an tested electronic device, thereby

increasing the reliability of the test by reducing test and device irregularities (see col. 3, lines 47-57).

**As per claims 2-4:**

Anand et al. in view of Thatcher et al. teach all the subject matter claimed in claim 1 including Anand et al. teach that the fuse controller has a standardized test interface protocol for an external tester includes a repair data processing unit adapted to initiate a BIST units. The invention has repair registers connected to the BIST units, which are adapted to collect repair data relating to the defective memory elements (arrays). The repair data processing unit determines lengths of the repair registers. The repair data processing reads and decompresses fuse data prior to initiating the BIST units. The repair data processing collects and compresses repair data after the BIST units test the memory elements. A fuse program count value is relayed to the tester, so that fuse programming time may be minimized. The fuses comprise e-fuses. Each of the fuses includes a fuse skip multiplexer adapted to cause fuses that are not to be programmed to be passed over during fuse programming (see col. 2, lines 14-61).

**As per claim 5:**

Anand et al. in view of Thatcher et al. teach all the subject matter claimed in claim 1 including Thatcher et al. teach that the first and second operating parameters 210 and 220 can include any electrical parameter, such as, input/output voltages, clock frequencies, etc. Furthermore, other embodiments are well suited to testing the

electronic device by varying other parameters that have an effect on the operating performance of the electronic device, such as, temperature, etc (see col. 4, lines 40-46).

**As per claims 6-9:**

Anand et al. in view of Thatcher et al. teach all the subject matter claimed in claim 1 including Anand et al. teach an invention that provides an application specific integrated circuit (ASIC) chip which has memory elements, a plurality of fuses connected to the memory elements that can be programmed to replace defective memory elements with replacement memory elements (arrays), and a fuse controller connected to the fuses that can program the fuses (see col. 2, lines 14-61). Further, Thatcher et al. teach that the first and second operating parameters 210 and 220 can include any electrical parameter, such as, input/output voltages, clock frequencies, etc. Furthermore, other embodiments are well suited to testing the electronic device by varying other parameters that have an effect on the operating performance of the electronic device, such as, temperature, etc (see col. 4, lines 40-46).

**As per claim 12:**

Anand et al. in view of Thatcher et al. teach all the subject matter claimed in claim 10 including Thatcher et al. teach that the first and second operating parameters 210 and 220 can include any electrical parameter, such as, input/output voltages, clock frequencies, etc. Furthermore, other embodiments are well suited to testing the electronic device by varying other parameters that have an effect on the operating performance of the electronic device, such as, temperature, etc (see col. 4, lines 40-46).

**As per claims 11 and 13-14:**

Anand et al. in view of Thatcher et al. teach all the subject matter claimed in claim 10 including Anand et al. teach that the repair data processing collects and compresses repair data after the BIST units test the memory elements. The repair data processing interrogates the actual compressed data to count the number of logical "ones" present (e.g., a count of the repairs needed), which represents the number of fuses needing to be programmed. A fuse program count value is relayed to the tester, so that fuse programming time may be minimized. The fuses comprise e-fuses. Each of the fuses includes a fuse skip multiplexer adapted to cause fuse that are not to be programmed to be passed over during fuse programming (see col. 2, lines 30-48).

**As per claims 15-20:**

Anand et al. in view of Thatcher et al. teach all the subject matter claimed in claim 1 including Anand et al. teach an invention that provides an application specific integrated circuit (ASIC) chip which has memory elements, a plurality of fuses connected to the memory elements that can be programmed to replace defective memory elements with replacement memory elements (arrays), and a fuse controller connected to the fuses that can program the fuses (see col. 2, lines 14-61). Further, Thatcher et al. teach that the first and second operating parameters 210 and 220 can include any electrical parameter, such as, input/output voltages, clock frequencies, etc. Furthermore, other embodiments are well suited to testing the electronic device by varying other parameters that have an effect on the operating performance of the electronic device, such as, temperature, etc (see col. 4, lines 40-46).

**Conclusion**

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US PN: 6230292 Duesman et al.

US PN: 5579266 Tahara et al.

Any inquiry concerning this communication or earlier communication from the examiner should be directed to Esaw Abraham whose telephone number is (571) 272-3812. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are successful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone numbers for the organization where this application or proceeding is assigned are (571) 273-8300 for regular communications and (571) 273-8300 for after final communications.

Information regarding the status of an Application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or PUBLIC PAIR. Status information for unpublished applications is available through Private Pair only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Esaw Abraham

Esaw Abraham

Art unit: 2133

GUY LAMARRE
PRIMARY EXAMINER